

CLAIMS

1. A variable-gain amplifier (VGA) comprising:

four first matched bipolar transistors arranged as an input pair and an output pair, each transistor connected at its base to the base of a corresponding transistor in the other pair;

an input-current source connected to the emitters of the input pair;

an output-current source connected to the emitters of the output pair;

a loop amplifier coupled between the collectors of the input pair and the connected bases of the input and output pairs, the loop amplifier comprising a gain transistor pair, each transistor in the gain pair having a base coupled to a corresponding input pair transistor collector;

a controllable gain-current source connected to the emitters of the gain pair; and

a gain-control circuit coupled to the gain-current source, the gain-control circuit adjusting the gain-current-source current such that the product of the input pair transconductance and the gain pair transconductance remains approximately constant.

2. The variable-gain amplifier of claim 1, wherein the gain-control circuit drives the input-current source and gain-current source to produce inversely related exponential currents.

3. The variable-gain amplifier of claim 2, the gain-control circuit comprising an external voltage interface, the gain-control circuit scaling VGA gain linearly in decibels as a function of the voltage V_G applied at the external voltage interface.

4. The variable-gain amplifier of claim 3, the gain-control circuit splitting a reference current I_P into two control currents I_{GD} and I_{GG} such that each varies linearly with V_G , but opposite each other, control current I_{GD} controlling the input-current source and control current I_{GG} controlling the gain-current source, wherein the input-current and gain-current sources each produce an output current that varies exponentially with control current.

5. The variable-gain amplifier of claim 4, the gain-control circuit comprising:

a gain-reference transistor pair sharing a temperature-stable tail current I_Z ;

a current-source-reference transistor pair sharing reference current I_P as a tail current, wherein I_P is proportional to absolute temperature, the gain control voltage used to shift current in the gain-reference pair, the gain-reference pair base-connected to the current

source-reference pair such that the current ratio at the gain-reference pair is reflected at the current source-reference pair; and

a gain-voltage amplifier that shifts a fraction z of tail current I_Z to one of the gain-reference transistors, the fraction z varying linearly with V_G .

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6. The variable-gain amplifier of claim 4, the gain-control circuit comprising a mode switch to allow gain to either increase or decrease with increasing V_G , the mode switch operating to swap I_{GD} and I_{GG} in order to switch modes.

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7. The variable-gain amplifier of claim 4, wherein the input-current source produces a temperature-stable tail current for the input pair, the tail current proportional to $I_D e^{I_{GG}/T}$, where T is absolute temperature, I_D is temperature-stable, and I_{GG} varies proportional to absolute temperature.

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8. The variable-gain amplifier of claim 7, wherein the gain-current source produces a tail current for the gain pair that is approximately proportional to the square of absolute temperature, the tail current proportional to $I_{SP} e^{-I_{GG}/T}$, where I_{SP} varies approximately with the square of absolute temperature.

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9. The variable-gain amplifier of claim 3, further comprising a second external voltage interface to an output-gain-control circuit, the output-gain-control circuit scaling amplifier gain linearly in magnitude as a function of the voltage V_{ML} applied to the second external voltage interface by varying the output pair tail current produced by the output current source linearly with V_{ML} .

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10. The variable-gain amplifier of claim 9, wherein the second external voltage interface is referenced to a bias voltage so as to set a default output gain when the second external voltage interface is left unconnected, and such that a voltage V_{ML} less than the bias voltage decreases the output gain below the default output gain and a voltage V_{ML} greater than the bias voltage increases the output gain above the default output gain.

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11. The variable-gain amplifier of claim 1, wherein the loop amplifier further comprises a Miller integrator coupled between the collectors of the gain pair and the connected bases of

the input and output pairs.

12. The variable-gain amplifier of claim 1, wherein the input-current source produces two matched input tail currents and the output-current source produces two matched output tail currents, one tail current for each of the four first matched bipolar transistors, the amplifier further comprising four second matched bipolar transistors, each sharing a common base and collector with a corresponding first matched bipolar transistor, each of the second transistors having its emitter connected to the matched tail current opposite that serving the corresponding first matched bipolar transistor.

13. The variable-gain amplifier of claim 12, wherein the four first transistors all have a first equal emitter area and the four second transistors all have a second equal emitter area different from the first size.

14. The variable-gain amplifier of claim 13, wherein the ratio of the first emitter area to the second emitter area is a ratio of two integers, each emitter implemented as an integer number of common-sized connected emitter regions.

15. The variable-gain amplifier of claim 12, further comprising eight collector-junction-capacitance (CJC)-cancellation transistors, each having its base-emitter junction shorted, each sharing a base connection with a corresponding one of the first and second bipolar transistors and matched in size to that corresponding transistor, each CJC-cancellation transistor collector cross-coupled to the opposite collector in the same pair as its corresponding transistor.

16. The variable-gain amplifier of claim 12, further comprising a two-terminal differential voltage input, each terminal coupled to a corresponding input pair collector by one of two matched resistors.

17. An integrated circuit comprising the variable gain amplifier of claim 1, the input pair and output pair transistors located substantially along a centerline of the integrated circuit and adjacent each other.

18. The integrated circuit of claim 17, substantially rectangular and comprising a number of bonding pads located along the circuit periphery, wherein bonding pad locations along each circuit edge are substantially mirrored along the opposite circuit edge.

5 19. A method of amplifying an input signal, the method comprising:

applying the signal as a differential current to the collectors of a first transistor pair having a first tail current;

mirroring the current densities in the first transistor pair to a second transistor pair having a second tail current by connecting the base of each transistor in the first pair to the
10 base of a corresponding transistor in the second pair;

driving the bases of the transistor pairs from a loop amplifier taking its input at the collectors of the first transistor pair;

adjusting the drive amplifier gain inversely proportional to changes in the transconductance of the first transistor pair, such that a loop gain for the drive amplifier
15 remains substantially constant; and

detecting an amplified signal as a differential current at the collectors of the second transistor pair.

20 20. The method of claim 19, further comprising adjusting the first tail current in response to a gain-setting signal.

21. The method of claim 20, wherein adjusting the first tail current comprises varying the first tail current exponentially for a linear change in the gain-setting signal.

25 22. The method of claim 21, wherein varying the first tail current exponentially and adjusting the drive amplifier gain inversely proportional comprises:

dividing a reference current into complementary first and second control currents;

applying the first control current as a control signal to a first exponential current generator that supplies the first tail current; and

30 applying the second control current as a control signal to a second exponential current generator that supplies a tail current to a differential current amplifier stage of the drive amplifier.

23. The method of claim 22, further comprising referencing the first exponential current generator to a temperature-stable base current, and referencing the second exponential current generator to a base current that varies proportional to the square of absolute temperature.

24. The method of claim 22, wherein varying the first tail current exponentially and adjusting the drive amplifier gain inversely proportional further comprises determining the division of the reference current by:

supplying a zero-temperature-coefficient gain-reference current;

steering a first portion of the gain-reference current to a first current branch by driving

the current in that current branch proportional to an input voltage;

steering the remaining portion of the gain-reference current to a second current branch; and

mirroring the division of gain-reference current between the first and second current branches to an equivalent division of the reference current between the first and second control currents.

25. The method of claim 22, further comprising accepting a mode signal, and swapping the first and second control currents when the mode signal is asserted, such that the first tail current decreases for a positive change in gain-setting signal in one mode, and the first tail current decreases for a positive change in gain-setting signal in another mode.

26. The method of claim 22, further comprising supplying a linear-in-magnitude control signal to a reference generator, and varying the second tail current proportional to the linear-in-magnitude control signal.